CLAIMS

1. (Currently Amended) A memory agent comprising:

a ~~first~~ receive link interface having a plurality of ~~first~~ receive lanes to receive training sequences; ~~and~~

a ~~second~~ transmit link interface having a plurality of ~~second~~ transmit lanes to transmit return sequences; and

~~wherein the memory agent is capable of selectively mapping one or more of the first lanes to one or more of the second lanes.~~

a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation.

2. (Currently Amended) [[A]] The memory agent according to claim 1 wherein:

the ~~first~~ receive link interface ~~comprises~~ is a first receive link interface; ~~and~~

the ~~second~~ transmit link interface ~~comprises~~ is a first transmit link interface[[.]];and further comprising:

a second transmit link interface having a plurality of second transmit lanes; and

a second receive link interface having a plurality of second receive lanes.

3. (Currently Amended) [[A]] The memory agent according to claim [[1]] 2 wherein[[:]]

~~the first lanes comprise receive bit lanes; and~~

~~the second lanes comprise transmit bit lanes.~~ the memory agent may operate in a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface.

4. (Currently Amended) [[A]] The memory agent according to claim 1 wherein the memory agent may selectively map one ~~or more~~ of the ~~first~~ receive lanes to ~~one or~~ more than one of the ~~second~~ transmit lanes during a lane testing operation.

5. (Currently Amended) [[A]] The memory agent according to claim 1 wherein the memory agent may selectively map one or more of the ~~first~~ receive lanes to one or more of the ~~second~~ transmit lanes according to a plurality of mappings.

6. (Currently Amended) [[A]] The memory agent according to claim [[1]] 5 wherein the memory agent may ~~selectively map one or more of the first lanes to one or more of the second lanes~~ select one of the mappings responsive to a mapping indicator in a training sequence received on the ~~first~~ receive link interface.

7. (Currently Amended) [[A]] The memory agent according to claim [[6]] 1 wherein the memory agent may retransmit the received training sequence with modification as the return sequence. ~~through the second link interface.~~

8. (Currently Amended) [[A]] The memory agent according to claim 1 wherein the memory agent comprises a memory buffer.

9. (Currently Amended) [[A]] The memory agent according to claim 1 wherein the memory agent comprises a memory module.

10. (Canceled)

11. (Currently Amended) [[A]] The memory agent according to claim 1 wherein the loopback unit comprises a multiplexer.

12. (Currently Amended) A memory agent comprising:

a first link interface having a plurality of first lanes; and

a second link interface having a plurality of second lanes;

wherein the memory agent may:

transmit training sequences having different mapping indicators on one or more of the plurality of first lanes;

receive return sequences on one or more of the plurality of second lanes responsive to the training sequences; and

~~analyzing~~ analyze the return sequences to identify failed lanes in the plurality of first lanes and the plurality of second lanes.

13. (Currently Amended) [[A]] The memory agent according to claim 12 wherein:

the first link interface comprises a receive link interface; and

the second link interface comprises a transmit link interface.

14. (Currently Amended) [[A]] The memory agent according to claim 12 wherein:

the first lanes comprise receive bit lanes; and

the second lanes comprise transmit bit lanes.

[[13]] 15. (Currently Amended) [[A]] The memory agent according to claim 12 wherein the memory agent may ~~identify whether a failed lane is a first lane or a second lane~~ receive the training sequences as the return sequences.

[[14]] 16. (Currently Amended) [[A]] The memory agent according to claim 12 wherein the memory agent may transmit test parameters in the training sequences.

[[15]] 17. (Currently Amended) [[A]] The memory agent according to claim 12 wherein the memory agent may transmit electrical stress patterns in the training sequences.

[[16]] 18. (Currently Amended) [[A]] The memory agent according to claim 12 wherein the memory agent comprises a memory controller.

[[17]] 19. (Currently Amended) A method comprising:

transmitting a first training sequence to a memory agent on a first plurality of lanes during a testing operation;

transmitting a first return sequence from the memory agent on a second plurality of lanes responsive to the first training sequence according to a first mapping during the testing operation;

transmitting a second training sequence to the memory agent on ~~a third~~ the first plurality of lanes during the testing operation; ~~and~~

transmitting a second return sequence from the memory agent on ~~a fourth~~ the second plurality of lanes responsive to the second training sequence according to a second mapping during the testing operation[[.]]; and

analyzing the return sequences based on the first and second mappings.

[[18]] 20. (Currently Amended) [[A]] The method according to claim [[17]] 19 ~~wherein the second plurality of lanes are the same as the fourth plurality of lanes.~~ further comprising:

redirecting the first training sequence to the second plurality of lanes as the first return sequence during the testing operation; and

redirecting the second training sequence to the second plurality of lanes as the second return sequence during the testing operation.

[[19]] 21. (Currently Amended) [[A]] The method according to claim [[18]] 20 ~~wherein the lanes comprise bit lanes.~~ further comprising:

passing the first training sequence through the memory agent to a third plurality of lanes during the testing operation;

passing the second training sequence through the memory agent to a third plurality of lanes during the testing operation;

passing the first return sequence from a fourth plurality of lanes through the memory agent to the second plurality of lanes during the testing operation; and

passing the second return sequence from the fourth plurality of lanes through the memory agent to the second plurality of lanes during the testing operation.

[[20]] 22. (Currently Amended) [[A]] The method according to claim [[17]] 19 wherein the first return sequence comprises one or more groups that are substantially the same as one or more groups in the first training sequence.

[[21]] 23. (Currently Amended) [[A]] The method according to claim [[17]] 19 wherein the second return sequence comprises one or more groups that are substantially the same as one or more groups in the second training sequence.

[[22]] 24. (Currently Amended) [[A]] The method according to claim [[17]] 19 wherein the first training sequence comprises a mapping indicator.

[[23]] 25. (Currently Amended) [[A]] The method according to claim [[17]] 19 wherein the first training sequence comprises an electrical stress pattern.

[[24]] 26. (Currently Amended) [[A]] The method according to claim [[17]] 19 wherein the memory agent comprises a memory module.

[[25]] 27. (Currently Amended) [[A]] The method according to claim [[17]] 19 wherein the memory agent comprises a memory buffer.

[[26]] 28. (Currently Amended) A memory system comprising:

memory agent comprising:

a ~~first~~ receive link interface having a plurality of ~~first~~ receive lanes to receive training sequences; ~~and~~

a ~~second~~ transmit link interface having a plurality of ~~second~~ transmit lanes to transmit return sequences; and

~~wherein the memory agent is capable of selectively mapping one or more of the first lanes to one or more of the second lanes.~~ a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation; and

a memory controller coupled to the memory agent.

[[27]] 29. (Currently Amended) [[A]] The memory ~~agent~~ system according to claim [[26]] 28 wherein:

the first link interface comprises a receive link interface; and

the second link interface comprises a transmit link interface.

[[28]] 30. (Currently Amended) [[A]] The memory ~~agent~~ system according to claim [[26]] 28 wherein:

the first lanes comprise receive bit lanes; and

the second lanes comprise transmit bit lanes.

[[29]] 31. (Currently Amended) [[A]] The memory system according to claim [[26]] 28 further comprising a second memory agent coupled to the memory agent.

32. (New) The memory agent according to claim 7 wherein the modification includes identifying or status information.

33. (New) The memory agent according to claim 1 wherein one of the return sequences comprises one of the received training sequences.

34. (New) The memory agent according to claim 1 wherein one of the return sequences consists essentially of one of the received training sequences.